B.E.(with Credits)-Regular-Semester 2012-Electronics & Telecommunication / Communication Engineering Sem III

ET 304 - Digital Electronics

P. Pages : 2 **GUG/S/18/3740**

Time : Three Hours * 0 8 9 9 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Due credit will be given to neatness and adequate dimensions.
3. Assume suitable data wherever necessary.
4. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) State and verify Demorgan's theorem. **4**

b) Reduce the following expression:- **6**

i) $(B+BC)\left(B+\overline{B}C\right)(B+D)$

ii) $AB+A\overline{B}C+B\overline{C}$

c) Solve using K-map **6**

i) $f(x, y, z) = \Sigma\,(0, 2, 4, 5, 6)$

ii) $f(A, B, C, D) = \Pi M\,(4, 6, 10, 12, 13, 15)$.

OR

2. a) Show that: **4**

i) $A \odot B = \overline{A} \odot \overline{B}$

ii) $\overline{A} \oplus B = A \oplus \overline{B} = A \odot B$.

b) Simplify using McClusky method. **8**

$f = \Sigma(1, 2, 5, 6, 7, 9, 10, 11, 14)$.

c) Simplify using K-map. **4**

$f\ (A\ B\ C\ D) = \Pi M\,(0, 2, 5, 9, 15)$

$d\,(6, 7, 8, 10, 12, 13)$

3. a) Define the following terms with reference to a logic gate: **8**

i) Propagation delay ii) Noise Margin

iii) Fan-in iv) Fan-out

b) Give the characteristics of TTL logic family. **8**

OR

4. a) Draw and explain 2 Input CMOS NAND gate. **8**

b) Explain I^2L & Compare with some important features of DTL. **8**

5. a) Draw & Explain BCD Adder. **8**

b) Implement a priority encoder with inputs D_0, D_1, D_2 and D_3. Assume D_3 having the highest and D_0 the lowest priority respectively. **8**

OR

6. a) Implement 4:1 multiplexer using NAND gate only. **8**

b) Implement 2-Bit magnitude Digital Comparator. **8**

7. a) Explain metastability in flip flop. **4**

b) Design a type T counter that goes through states 0, 3, 5, 6, 0. If the counter suffers the problem of lockout redesign the counter assuming that the counter goes to the starting state i.e. 000 if it enters any invalid state. **12**

OR

8. a) In a 4-stage ripple counter, the propagation delay of a flip flop is 50nsec. If the pulse width of the strobe is 30nsec. Find the maximum frequency at which the counter operates. **4**

b) Draw 4-Bit Ring counter using D Flip Flop and show its waveform. **6**

c) Design JK Flip Flop using SR Flip Flop. **6**

9. a) Explain FPGA Architecture with diagram. **8**

b) Draw & Explain 1-Bit memory cell with three terminal namely Read/Write $\left(R/\overline{W}\right)$, Address enable (AE) and data in/data out. **8**

OR

10. a) Draw & Explain Bipolar static RAM. **8**

b) Write short note on: **8**
i) Flash memory ii) CPLD

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